

IMAGE PROCESSING APPARATUS

FIELD OF THE INVENTION

The present invention in general relates to an image
5 processing apparatus. More specifically, this invention
relates to an image processing apparatus that reads both
the surfaces of a document and performs specific image
processing.

10 BACKGROUND OF THE INVENTION

Various kinds of image processing apparatuses are
known. In recent years, there has been an image processing
apparatus capable of processing a double-sided document
having images printed on both sides thereof in consideration
15 of environment. When information written in a double-sided
document is filed in a double-sided copying machine or a
double-sided electronic filing apparatus, the document is
read by an image reader such as an image scanner.

In order to compensate the function of reading only
20 either side of a document in a simple image reader, the
document is turned over by an operator after the obverse
of the document is read, and then, the reverse of the document
is read. Otherwise, in a simple double-sided image reader,
a document is turned over by a mechanical mechanism after
25 the obverse of the document is read, and subsequently, the

reverse of the document is read.

However, the image reader which reads only either side of a document places a significant burden on a user, and further, inconveniently takes much time to read the document.

5 In the meantime, in the double-sided image reader having a mechanical turning-over function, there may accidentally occur drawbacks caused by the mechanical mechanism, for example, paper jamming in turning-over, or mechanical failures. In order to eliminate such inconveniences, there
10 has been known an image processing apparatus including respective readers for both of the obverse and the reverse of a document, in which the readers simultaneously read images of the obverse and the reverse of the document. The use of such an image reader can achieve image processing
15 of double-sided copying or the like at a high speed with few failures.

Now, a digital combined machine having a double-sided copying function will be explained as one example of conventional image processing apparatuses for performing
20 double-sided reading. Fig. 15 is a block diagram illustrating one example of the configuration of a conventional double-sided copying machine. As illustrated in Fig. 15, the digital combined machine comprises a series of constituent units such as a reading unit 1501, an image
25 processing unit 1502, a video controller 1503 and a writing

unit 1504; component elements constituting a copying machine
(i.e., the section of a copying machine) consisting of a
memory control unit 1505 and a memory module 1506; a process
controller 1511, a RAM 1512 and a ROM 1513; and various units
5 such as a facsimile control unit 1512, a printer control
unit 1513 and a scanner control unit 1514 which are
additionally connected via a motherboard 1511.

The motherboard 1511 is constituted of an obverse image
transfer bus 1515a for transferring obverse image data and
10 a reverse image transfer bus 1515b for transferring reverse
image data. These buses are normally required to transfer
image data, which are simultaneously read by the reading
unit 1501, at the same timing with the same data structure.
Furthermore, the two image transfer buses are required also
15 to input the image data on both sides of a document read
by the scanner control unit 1514 installed externally.

The reading unit 1501 is constituted of an obverse
reading unit 1501a for reading the obverse of the document
and a reverse reading unit 1501b for reading the reverse
20 of the document. In the same manner, the image processing
unit 1502 is constituted of an obverse image processing unit
1502a and a reverse image processing unit 1502b.
Furthermore, the video controller 1503 is constituted of
an obverse video controller 1503a and a reverse video
25 controller 1503b.

When both sides of the document are read in the image processing apparatus, the volume of the image data input at the same time is twice in comparison with that in the image processing apparatus which reads only either side of the document. Consequently, the read image data is compressed such that the image data is efficiently stored in the memory module 1506 or the image data is efficiently transferred via the various buses.

How the image data is compressed will be explained here. Fig. 16 is a block diagram illustrating one example of the configuration of a data compressor in the memory control unit 1505; and Fig. 17 is a timing chart illustrating the processing timings thereof.

In Fig. 16, the data compressor 1601 comprises: an obverse storage 1602a and a reverse storage 1602b for storing therein obverse image data and reverse image data, respectively; an obverse compressor 1603a and a reverse compressor 1603b for compressing the obverse image data and the reverse image data, respectively; and a controller 1604 for controlling the obverse storage 1602a, the reverse storage 1602b, the obverse compressor 1603a and the reverse compressor 1603b.

The alphabetic subscripts a and b will hereinafter designate constituent elements relevant to the obverse image data and the reverse image data, respectively, wherein they

are not attached when they need not be specially distinguished from each other.

The storage 1602 includes a line memory group 1605 consisting of a plurality of 1-port FIFO memories FM1, FM2, FM3, FM4 and FM5; an output switch 1606 for switching the output destination of the image data; and an input switch 1607 for switching the input source of the image data between the FIFO memories FM1 and FM2.

Incidentally, for the sake of simple explanation, a region to be compressed by the compressor 1603 is assumed to be a rectangular region consisting of four pixels per line multiplied by four lines, that is, four pixels in a main scanning (pixel) direction and four lines in a sub scanning (line) direction, as illustrated in Fig. 18.

As illustrated in Fig. 17, with respect to the compression of image data on the obverse, image data on a first line in the rectangular region of the obverse is written in the FIFO memory FM1a. Next, image data on a second line is written in the FIFO memory FM3a; image data on a third line is written in the FIFO memory FM4a; and image data on a fourth line is written in the FIFO memory FM5a, in sequence. The image data at this time is divided by the obverse output switch 1606a under the control of the controller 1604.

In the stage in which the image data is written in the FIFO memory FM5a, there appear all of the four lines

to be compressed by the obverse compressor 1603a. Subsequently, the image data on the first to fourth lines stored in the FIFO memories FM1a, FM3a, FM4a and FM5a, respectively are read out, to be transmitted to the obverse
5 compressor 1603a. This transmission is controlled by the controller 1604. The obverse compressor 1603a compresses the image data on the four lines as a single unit, and then, outputs the compressed image data. The compressed image data is then stored in the memory module 1506.

10 In the meantime, after the image data on the fourth line is written in the FIFO memory FM5a, image data on a first line in a next rectangular region (i.e., image data on a fifth line) of the obverse is input. The controller 1604 controls to write the image data on the fifth line in
15 the FIFO memory FM2a in order to avoid a memory conflict.

Thereafter, image data on a sixth line is written in the FIFO memory FM3a; image data on a seventh line is written in the FIFO memory FM4a; and image data on an eighth line is written in the FIFO memory FM5a, in sequence.

20 The controller 1604 reads the image data on the fifth to eighth lines stored in the FIFO memories FM2a to FM5a, respectively, to thus transmit them to the obverse compressor 1603a, while controlling to write image data on a ninth line in a next rectangular region in the FIFO memory FM1a. A
25 series of sequentially input image data on the obverse can

be compressed without any hitch by repeating the above-described processing.

In the meanwhile, the image data on the reverse of the document also is input into the data compressor 1601 together with the image data on the obverse. Since the processing of the image data on the reverse is the same as that of the image data on the obverse, the explanation thereof will be omitted here. Compressing operation is repeated every four lines under the control of the controller 1604, so that a series of sequentially input image data on the reverse can be compressed without any hitch.

In this way, since double processing is required in comparison with the processing of the data on either one side when the image data on both sides of the document are input, the data compressing processing has become an important factor for the performance of the apparatus including ease of use of the apparatus. In other words, the conventional image processing apparatus for performing double-sided reading is provided with two compressors for the obverse image data and the reverse image data, for inputting the image data on the obverse and the reverse at a high speed and efficiently transferring and storing the data.

Furthermore, as an apparatus for performing double-sided reading has been devised an apparatus for

effectively using a reverse image processing unit block in reading one side of a document which has an image only at the obverse ("an image reader" disclosed in Japanese Patent Application Laid-Open (JP-A) No. 10-336396).

5 However, the conventional image processing apparatus for performing double-sided reading at the same time must be provided with two compressors and two data buses for the obverse and the reverse. Thus, there has arisen a problem of the unwieldy size of a processing circuit.

10 In particular, in a digital combined machine in which functional units are provided independently of each other and they can be replaced when the function is enhanced, the size of the machine need be reduced as possible in view of the configuration of the machine.

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SUMMARY OF THE INVENTION

It is an object of the present invention to provide an image processing apparatus in which the size of a processing circuit can be reduced, and further, both of the obverse and reverse of a document can be read at the same time.

20 The image processing apparatus according to one aspect of the present invention has a reading unit which simultaneously reads image data from two, an obverse and a reverse, surfaces of a document; a compressing unit which

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compresses received image data. The image processing apparatus further comprises a controlling unit which orchestrates a flow of image data from the reading unit to the compressing unit in such a manner that the image data
5 corresponding to the obverse surface and the reverse surface is input into the compressing unit at different timing. Thus, the processing circuit can be shared by shifting the timings of the image processing of the obverse image data and the image processing of the reverse image data.

10 The image processing apparatus according to another aspect of the present invention comprises a reading unit which simultaneously reads image data from two, an obverse and a reverse, surfaces of a document; a storing unit which receives and stores therein the image data read by the reading
15 unit; a compressing unit which receives and compresses the image data stored in the storing unit; and a controlling unit which orchestrates compression of the image data stored in the storing unit by the compressing unit in such a manner that the image data corresponding to the obverse surface
20 and the reverse surface is compressed at different timing. Thus, it becomes possible to compress the obverse and reverse image data with only one compressing unit.

The image processing apparatus according to still another aspect of the present invention comprises a reading
25 unit which simultaneously reads image data from two, an

obverse and a reverse, surfaces of a document; a data dividing unit which divides the image data acquired by the reading unit from the obverse surface and reverse surface respectively into image data of $m \times n$ pixels, where n is the number of lines and m is the number of pixels in one line, and $n < N$ and $m < M$ where N is the maximum number of scan lines, and M is the maximum number of pixels in one lines; a storing unit which receives the image data of first $m \times (n-1)$ pixels, corresponding to the obverse surface and the reverse surface, from the data dividing unit, and stores the data therein; a compressing unit which receives the image data of $m \times n$ pixels and compresses the image data as a single unit; a switch unit which controls a flow of the image data from the storing unit to the compressing unit, wherein the switch unit allows either the image data corresponding to the obverse surface or the reverse surface to be input into the compressing unit at one time; and a transmission controlling unit which controls a flow of the image data from the data dividing unit to the storing unit and to the compressing unit, wherein the transmission controlling unit allows the image data of first $m \times (n-1)$ pixels from the data dividing unit to be input into the storing unit, and allows the image data of last m pixels from the data dividing unit to be directly input into the compressing unit. Thus, it becomes possible to compress the obverse and reverse image

data with only one compressing unit. Further, since image data corresponding only to $m \times (n-1)$ pixels is stored in storing unit, it becomes possible to reduce memory size of the storing unit and thereby reduce the cost.

5 The image processing apparatus according to still another aspect of the present invention comprises a reading unit which simultaneously reads image data from two, an obverse and a reverse, surfaces of a document; an appending unit which receives the image data acquired by the reading
10 unit appends identifying information to the image data for identifying whether the image data corresponds to the obverse surface or to the reverse surface; and a communication line to be used to send the identifying information appended image data corresponds to the obverse surface and the reverse
15 surface; an obverse image processing unit which obtains, based on the appended identifying information, only the image data corresponding to the obverse surface from the communication line, and performs specific image processing to the obtained image data; and a reverse image processing
20 unit which obtains, based on the appended identifying information, only the image data corresponding to the reverse surface from the communication line, and performs specific image processing to the obtained image data. Thus, it becomes possible to identify whether the image data read
25 by the reading unit is the obverse image data or the reverse

image data, and to transmit or receive the obverse and reverse image data via the same data bus without any necessity of providing a data bus for each of the obverse processing and the reverse processing.

5 Other objects and features of this invention will become apparent from the following description with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

10 Fig. 1 is a block diagram functionally illustrating the arrangement of an image processing apparatus in a first embodiment according to the present invention;

 Fig. 2 is a block diagram illustrating one example of the hardware configuration of the image processing
15 apparatus in the first embodiment;

 Fig. 3 is a block diagram illustrating the outline of processing in an image processor in the image processing apparatus in the first embodiment;

 Fig. 4 is a block diagram illustrating the outline
20 of the processing in an image data controller in the image processing apparatus in the first embodiment;

 Fig. 5 is a block diagram illustrating the outline of the processing in a video data controller in the image processing apparatus in the first embodiment;

25 Fig. 6 is a block diagram illustrating the outline

of the processing in an image memory access controller 221
in the image processing apparatus in the first embodiment;

Fig. 7 is a block diagram illustrating the
configuration of a facsimile control unit in the image
5 processing apparatus in the first embodiment;

Fig. 8 is a block diagram illustrating one example
of unit configuration when the image processing apparatus
is a digital combined machine;

Fig. 9 is a block diagram illustrating the
10 configuration of a data compressor in the image processing
apparatus in the first embodiment;

Fig. 10 is a timing chart illustrating the processing
timings of the data compressor illustrated in Fig. 9;

Fig. 11 is a block diagram illustrating another example
15 of the configuration of the image processing apparatus when
a single image processor is used;

Fig. 12 is a block diagram illustrating one example
of the configuration of the image processor illustrated in
Fig. 11;

20 Fig. 13 is a block diagram illustrating one example
of the hardware configuration of an image processing
apparatus in a second embodiment;

Fig. 14A and Fig. 14B illustrate image data added with
identifying data;

25 Fig. 15 is a block diagram illustrating one example

of the configuration of a conventional double-sided copying machine;

Fig. 16 is a block diagram illustrating one example of the configuration of a data compressor in a conventional memory control unit;

Fig. 17 is a timing chart illustrating the processing timings of the data compressor illustrated in Fig. 16; and

Fig. 18 illustrates one example of image data to be compressed by the data compressor.

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DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the image processing apparatus according to the present invention will be described below in reference to the drawings.

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The principle of the image processing apparatus which is common to all the embodiments will be explained here. Fig. 1 is a block diagram functionally illustrating the arrangement of the image processing apparatus in the preferred embodiment according to the present invention.

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The image processing apparatus includes five units.

That is, the image processing apparatus includes an image data control unit 100; an image reading unit 101 for reading and inputting image data; an image memory control unit 102 for controlling an image memory for storing an image therein so as to write/read the image data; an image

processing unit 103 for subjecting the image data to image processing such as edition; and an image writing unit 104 for writing the image data in a transfer sheet or the like.

The above-described units are arranged centering on
5 the image data control unit 100: namely, the image reading unit 101, the image memory control unit 102, the image processing unit 103 and the image writing unit 104 are connected to the image data control unit 100.

The image data control unit 100 undertakes, for example,
10 following processing:

(1) data compressing processing (primary compression) for the purpose of enhancing the bus transfer efficiency of data;

(2) processing of transferring the primarily
15 compressed data to image data;

(3) image synthesizing processing (which enables image data from a plurality of units to be synthesized, and further, includes synthesizing the image data on a data bus);

(4) image shifting processing (which enables an image
20 to be shifted in main and sub scanning directions);

(5) image region expanding processing (which enables an image region to be magnified to the periphery by an arbitrary amount);

(6) image scaling processing (to, for example, a fixed
25 scale of 50% or 200%);

- (7) parallel bus interface processing;
- (8) serial bus interface processing (with a process controller 211, described later);
- (9) format converting processing between parallel
5 data and serial data;
- (10) interface processing with the image reading unit
101;
- (11) interface processing with the image processing
unit 103; and
- 10 (12) data decompressing processing.

The image reading unit 101 undertakes, for example,
following processing:

- (1) processing of reading light reflected on an
original by means of an optical system;
- 15 (2) processing of converting the light into an
electric signal in a CCD (a charge coupled device);
- (3) digitizing processing by means of an A/D
(analog-to-digital) converter;
- (4) shading correcting processing (processing of
20 correcting unevenness of illumination distribution of a
light source); and
- (5) scanner γ correcting processing (processing of
correcting the concentration characteristics of a reading
system).

25 The image memory control unit 102 undertakes, for

example, following processing:

(1) interface control processing with a system controller;

(2) parallel bus control processing (processing of
5 controlling an interface with a parallel bus);

(3) network control processing;

(4) serial bus control processing (processing of
controlling a plurality of outside serial ports);

(5) inside bus interface control processing
10 (processing of controlling a command with respect to an
operating unit);

(6) local bus control processing (processing of
controlling accesses of the ROM, the RAM and font data for
booting the system controller);

(7) processing of controlling operation of a memory
15 module (processing of controlling a writing/reading
operation of a memory module);

(8) memory module access control processing
(processing of conciliating requests for a memory access
20 from a plurality of units);

(9) obverse and reverse image data
compressing/decompressing processing (processing of
reducing the amount of data for the purpose of memory
effective use);

(10) image editing processing (processing of clearing
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data in a memory region, turning the image data, synthesizing images on a memory, and the like) ; and

(11) processing of controlling inputting of obverse and reverse image data to be input from a reading unit.

5 The image processing unit 103 undertakes, for example, following processing:

(1) shading correcting processing (processing of correcting unevenness of illumination distribution of a light source);

10 (2) scanner γ correcting processing (processing of correcting the concentration characteristics of a reading system);

(3) MTF correcting processing;

(4) smoothing processing;

15 (5) arbitrarily scaling processing in a main scanning direction;

(6) concentration varying processing (γ varying processing: a concentration notch);

(7) simple multi-level processing;

20 (8) simple binary processing;

(9) error diffusing processing;

(10) dithering processing;

(11) dot arrangement phase control processing (processing of arranging dots rightward or leftward);

25 (12) isolated point eliminating processing;

(13) image region separating processing (color judgment, attribute judgment or adaptation); and

(14) density varying processing.

The image writing unit 104 undertakes, for example,
5 following processing:

(1) edge trimming processing (shagginess correcting processing);

(2) dot re-arrangement correcting processing;

(3) processing of controlling a pulse of an image
10 signal; and

(4) processing of converting a format of parallel data or serial data.

Next, hardware configuration in which the image processing apparatus 105 in the present embodiment
15 constitutes a digital combined machine will be explained. Fig. 2 is a block diagram illustrating one example of the hardware configuration of the image processing apparatus in the present embodiment. Hereinafter, an alphabet a is attached to components for processing the obverse image data;
20 another alphabet b is attached to components for processing the reverse image data; and no alphabet is attached when components are generically called.

In the block diagram illustrated in Fig. 2, the image processing apparatus in the present embodiment comprises
25 an obverse reading unit 201a, a reverse reading unit 201b,

an obverse sensor board unit 202a, a reverse sensor board unit 202b, an image data controller 203, an obverse image processor 204a, a reverse image processor 204b, a video data controller 205 and an image forming unit (engine) 206. The
5 image processing apparatus in the present embodiment further comprises a process controller 211, a RAM 212 and a ROM 213 via a serial bus 210.

Moreover, the image processing apparatus in the present embodiment comprises an image memory access
10 controller 221 and a facsimile control unit 224 via a parallel bus 220, and a memory module 222, a system controller 231, a RAM 232, a ROM 233 and a console panel 234, all of which are connected to the image memory access controller 221.

The correlation between the above-mentioned
15 constituent elements and the units 100 to 104 illustrated in Fig. 1 will be explained. Namely, the reading unit 201 and the sensor board unit 202 fulfill the function of the image reading unit 101 illustrated in Fig. 1. In the same manner, the image data controller 203 serves the function
20 of the image data controller unit 100. Furthermore, in the same manner, the image processor 204 carries out the function of the image processing unit 103.

Moreover, in the same manner, the video data controller 205 and the image forming unit (engine) 206 fulfill the
25 function of the image writing unit 104. Additionally, in

the same manner, the image memory access controller 221 and the memory module 222 serve the function of the image memory control unit 102.

Next, the contents of the constituent elements will
5 be explained. The reading unit 201 for optically reading an original is constituted of a lamp, mirrors and lenses, in which light reflected on the original with irradiation by the lamp is focused on a light receiving element by the mirrors and the lenses. In the present embodiment, the image
10 data are obtained from the obverse and reverse of the document, and therefore, the lamps, the mirrors and the light receiving elements are required in twos.

The light receiving element, for example, a CCD, is mounted on the sensor board unit 202. Image data converted
15 into an electric signal by the CCD is further converted into a digital signal, to be then output (transmitted) from the sensor board unit 202.

The image data output (transmitted) from the sensor board unit 202 is input into (received by) the image data
20 controller 203. All the transmission of the image data between the functional devices (the processing units) and the data buses is controlled by the image data controller 203.

The image data controller 203 transfers the image data
25 to the sensor board unit 202, the parallel bus 220 and the

image processor 204, and transmits the image data to the process controller 211 and the system controller 231 which manages the entire control of the image processing apparatus. Moreover, the RAM 212 is used as a work area of the process controller 211, and the ROM 213 stores therein a boot program for the process controller 211, and the like.

The image data output (transmitted) from the sensor board unit 202 is compressed with respect to the obverse or reverse, as required, to be thus transferred (transmitted) to the image processor 204 via the image data controller 203, and thereafter, deterioration of the signal associated with quantization to the optical system and a digital signal (i.e., deterioration of the signal in the scanner system) is corrected, thereby outputting (transmitting) the image data to the image data controller 203 again.

The image memory access controller 221 controls writing/reading of the image data in/from the memory module 222. Furthermore, the image memory access controller 221 controls the operation of each of the constituent elements connected to the parallel bus 220. Moreover, the RAM 232 is used as a work area of the system controller 231. The ROM 233 stores therein the boot program and the like for the system controller 231.

The console panel 234 inputs the processing to be performed by the image processing apparatus 105: for

example, the kind of processing (copying, facsimile transmission, image reading, printing or the like), the number of sheets to be processed or the like. Consequently, it is possible to input image data control information.

5 Incidentally, the content of the facsimile control unit 224 will be described later.

Subsequently, there are a job for accumulating the read image data in the memory module 222 for reuse and a job for not accumulating the read image data in the memory module 222. Now, each of the jobs will be explained below.

10 As an example of the job for accumulating the read image data in the memory module 222, there is a method in which when a single original is copied onto a plurality of sheets, the reading unit 201 is operated only once, and then, the

15 image data read by the reading unit 201 is accumulated in the memory module 222, and therefore, the accumulated image data is read out a plurality of times.

In contrast, as an example of the job for not accumulating the read image data in the memory module 222,

20 when a single original is copied onto only one sheet, the read image data is simply reproduced as it is, and consequently, no access is required to the memory module 222 by the image memory access controller 221.

First of all, when the memory module 222 is not used,

25 the data transferred from the image processor 204 to the

image data controller 203 is returned again to the image processor 204 from the image data controller 203. The image processor 204 performs image quality processing for converting luminance data obtained by the CCD in the sensor board unit 202 into an area gradation.

The image data after the image quality processing is transferred from the image processor 204 to the video data controller 205. The signal, which has been converted into the area gradation, is subjected to post-processing relating to dot arrangement and pulse control for reproducing dots, and thereafter, a reproduced image is formed on a transfer sheet in the image forming unit 206.

Subsequently, flow of the image data when additional processing, for example, a turn in an image direction, synthesis of images or the like is performed in reading the image accumulated in the memory module 222 will be explained. The image data transferred to the image data controller 203 from the image processor 204 is transmitted to the image memory access controller 221 from the image data controller 203 via the parallel bus 220.

The image memory access controller 221 performs access control of the image data by the memory module 222, development of printing data in an outside personal computer (PC) 223, and compression/decompression of the image data for effective use of the memory module 222 based on the control

of the system controller 231.

The image data transmitted to the image memory access controller 221 is accumulated in the memory module 222 after data compression, and the accumulated image data is read, as required. The read image data is decompressed to the original image data, and then, is returned to the image data controller 203 from the image memory access controller 221 via the parallel bus 220.

After the transmission from the image data controller 203 to the image processor 204, the image quality processing and the pulse control in the video data controller 205 are performed, thereby forming a reproduced image on a transfer sheet in the image forming unit 206.

In the flow of the image data, the function of the digital combined machine can be served under the bus control in the parallel bus 220 and the image data controller 203. In order to exhibit the facsimile transmission function, the read image data is subjected to the image processing in the image processor 204, and then, is transferred to the facsimile control unit 224 via the image data controller 203 and the parallel bus 220. The facsimile control unit 224 performs data conversion with respect to a communication network, and then, transmits the data as facsimile data to a public network (PN) 225.

In the meantime, as to the received facsimile data,

network data from the public network (PN) 225 is converted into image data in the facsimile control unit 224, and then, is transferred to the image processor 204 via the parallel bus 220 and the image data controller 203. In this case, dot rearrangement and the pulse control are performed in the video data controller 205, and thereafter, a reproduced image is formed on a transfer sheet in the image forming unit 206.

When the plurality of jobs, for example, the copying function, the facsimile transmitting/receiving function, the printer outputting function and the like are performed simultaneously, the assignment of the using priority of the image forming unit 206 and parallel bus 220 to the jobs is controlled by the system controller 231 and the process controller 211.

The process controller 211 controls the flow of the image data; in contrast, the system controller 231 controls the entire system and manages the booting of resources. Furthermore, the functions of the digital combined machine are selectively input in the console panel (the operating unit) 234, and thus, the processing content of the copying function, the facsimile function or the like is set.

The system controller 231 and the process controller 211 communicate with each other via the parallel bus 220, the image data controller 203 and the serial bus 210.

Specifically, the system controller 231 and the process
controller 211 communicate with each other by converting
a data format for a data interface between the parallel bus
220 and the serial bus 210 inside the image data controller
5 203.

Next, an outline of the processing in the image
processor 204 constituting the image processing unit 103
will be explained. Fig. 3 is a block diagram illustrating
the outline of the processing in the image processor 204
10 in the image processing apparatus in the present embodiment.
Although the image processor 204 includes an obverse image
processor 204a for processing obverse image data and a
reverse image processor 204b for processing reverse image
data, an explanation will be given without specifically
15 distinguishing the obverse image processor 204a and the
reverse image processor 204b from each other.

In the block diagram of Fig. 3, the image processor
204 includes a first input interface (I/F) 301, a scanner
image processor 302, a first output I/F 303, a second input
20 I/F 304, an image quality processor 305 and a second output
I/F 306.

In the above-mentioned configuration, read image data
is transmitted from the first input I/F 301 to the scanner
image processor 302 in the image processor 204 via the sensor
25 board unit 202 and the image data controller 203.

The scanner image processor 302 is directed to correct the deterioration of the read image data: specifically, shading correction, scanner γ correction, MTF correction and the like. Furthermore, the scanner image processor 302
5 can perform scaling processing of enlargement/reduction, although not the correction processing in the strict sense. Upon completion of the correction processing of the read image data, the image data is transferred to the image data controller 203 via the first output interface 303.

10 In outputting the image data to a transfer sheet, the image data from the image data controller 203 is received in the second input I/F 304, and then, is subjected to the area gradation processing in the image quality processor 305. The image data after the image quality processing is
15 output to the video data controller 205 or the image data controller 203 via the second output I/F 306.

The area gradation processing in the image quality processor 305 includes mainly area approximation of gradation information such as density converting processing,
20 dither processing and error diffusing processing. Once the image data processed in the scanner image processor 302 is accumulated in the memory module 222, various reproduced images can be confirmed by changing the image quality processing in the image quality processor 305.

25 For example, the tone of the reproduced image can be

easily varied by assigning (varying) the density of the reproduced image or varying the number of lines of dither matrices. At this time, it is unnecessary to read the image from the reading unit 201 every time the processing is varied.

5 The same image data can be speedily subjected to different processing any time by reading the accumulated image data from the memory module 222.

Next, an outline of the processing in the image data controller 203 constituting the image data control unit 100
10 will be explained. Fig. 4 is a block diagram illustrating the outline of the processing in the image data controller 203 in the image processing apparatus in the present embodiment.

As illustrated in the block diagram of Fig. 4, an image
15 data input/output controller 401 inputs (receives) the image data from the sensor board unit 202, and then, outputs (transmits) the image data to the image processor 204. That is, the image data input/output controller 401 is a constituent element for connecting the image reading unit
20 101 and the image processing unit 103 (the image processor 204) to each other, or an input/output port exclusive for merely transmitting the image data read by the image reading unit 101 to the image processing unit 103.

Furthermore, an obverse image data input controller
25 402a inputs the image data, which has undergone scanner image

correction in the obverse image processor 204a. The input
image data is subjected to data compressing processing in
a data compressor 403. Thereafter, the image data is sent
to the parallel bus 220 through a parallel data I/F 405 via
5 a data converter 404.

In a similar manner, a reverse image data input
controller 402b inputs the image data, which has undergone
scanner image correction in the reverse image processor 204b.
The input image data is subjected to data compressing
10 processing in the data compressor 403. Thereafter, the
image data is sent to the parallel bus 220 through the parallel
data I/F 405 via the data converter 404. The configuration
and operation of the data compressor 403 will be described
later in detail.

15 Since the image data input from the parallel bus 220
via the parallel data I/F 405 is compressed for the purpose
of the bus transfer, the image data is sent to a data
decompressor 406 via the data converter 404, to be thus
subjected to data decompressing processing. The
20 decompressed image data is transferred to the image processor
204 in an image data output controller 407.

Moreover, the image data controller 203 is also
equipped with the function of converting parallel data into
serial data, and vice versa. The system controller 231
25 transfers the data to the parallel bus 220; in the meantime,

the process controller 211 transfers the data to the serial bus 210. Therefore, the image data controller 203 converts the data for the purpose of the communications between the two controllers.

5 Additionally, a serial data I/F unit includes a first serial data I/F 408 for transmitting or receiving the data to or from the process controller via the serial bus 210 and a second serial data I/F 409 for use in transmitting or receiving the data to or from the image processor 204.
10 Since one system is independently provided with respect to the image processor 204, it is possible to smoothen an interface with the image processor 204.

 Furthermore, a command controller 410 controls the operations of the constituents and interfaces inside the
15 above-described image data controller 203 in accordance with an input command. The command controller 410 controls the operation of, in particular, a data compressing/decompressing unit 411 including the data compressor 403 and the data decompressor 406. The control will be described
20 later in detail.

 Next, an outline of the processing in the video data controller 205 constituting a part of the image writing unit 104 will be explained. Fig. 5 is a block diagram illustrating the outline of the processing in the video data controller
25 205 in the image processing apparatus in the present

embodiment.

As illustrated in the block diagram of Fig. 5, the video data controller 205 subjects the image data to be input to additional processing depending upon the characteristics of the image forming unit 206. Namely, an edge trimming processor 501 rearranges dots by edge trimming processing. A pulse controller 502 controls a pulse of an image signal for the purpose of dot formation. The image data through the above-described processing is output to the image forming unit 206.

Besides the image data conversion, since the video data controller 205 is equipped with the format converting function for parallel data and serial data, the video data controller 205 even as a discrete unit can cope with the communications between the system controller 231 and the process controller 211. That is, a parallel data I/F 503 for transmitting or receiving the parallel data, a serial data I/F 504 for transmitting or receiving the serial data and a data converter 505 for mutually converting the data received by the parallel data I/F 503 and the data received by the serial data I/F 504. Consequently, it is possible to convert the format of the parallel data into the format of the serial data, and vice versa.

Next, an outline of the processing in the image memory access controller 221 constituting a part of the image memory

control unit 102 will be explained. Fig. 6 is a block diagram illustrating the outline of the processing in the image memory access controller 221 in the image processing apparatus in the present embodiment.

5 As illustrated in the block diagram of Fig. 6, the image memory access controller 221 manages the parallel bus 220 and the interface of the image data, controls an access, i.e., storing (writing)/reading of the image data in the memory module 222, and further, controls development of code data to be input from mainly the outside PC 223 to the image data.

Therefore, the image memory access controller 221 includes a parallel data I/F 601, a system controller I/F 602, a memory access controller 603, a line buffer 604, a video controller 605, a data compressor 606, a data decompressor 607 and a data converter 608.

Here, the parallel data I/F 601 manages an interface of the image data with the parallel bus 220. Furthermore, the memory access controller 603 controls an access, i.e., storing (writing)/reading of the image data in the memory module 222.

As to the input code data, the data is stored in a local region in the line buffer 604. The code data stored in the line buffer 604 is developed to image data in the video controller 605 in accordance with a development

processing command input from the system controller 231 via the system controller I/F 602.

The developed image data or the image data input from the parallel bus 220 via the parallel data I/F 601 is stored in the memory module 222. In this case, the image data to be stored is selected in the data converter 608, to be thus compressed in the data compressor 606 in order to enhance memory using efficiency, and then, the image data is stored (written) in the memory module 222 while an address of the memory module 222 is managed in the memory access controller 603.

The image data stored (accumulated) in the memory module 222 is read by controlling an address to be read in the memory access controller 603. The read image data is decompressed in the data decompressor 607. In the case where the decompressed image data is transferred to the parallel bus 220, the data is transferred via the parallel data I/F 601.

Next, functional configuration of the facsimile control unit 224 will be explained. Fig. 7 is a block diagram illustrating the configuration of the facsimile control unit 224 in the image processing apparatus in the present embodiment.

As illustrated in the block diagram of Fig. 7, the facsimile control unit 224 comprises a facsimile

transmitter/receiver 701 and an outside I/F 702. Here, the facsimile transmitter/receiver 701 converts image data into a format for the communications, so as to transmit it to an outside network; in contrast, the facsimile transmitter/receiver 701 converts data from the outside into image data so as to record and output it in the image forming unit via the outside I/F 702 and the parallel bus 220.

The facsimile transmitter/receiver 701 includes a facsimile image processor 703, an image memory 704, a memory controller 705, a data controller 706, an image compressor/decompressor 707, a modem 708 and a network controller 709.

In the facsimile image processor 703, binary smoothing processing with respect to a received image is performed in the edge trimming processing 501 inside the video data controller 205 illustrated in Fig. 5. In the image memory 704, a part of an output buffer function is shifted to the image memory access controller 221 and the memory module 222.

In the facsimile transmitter/receiver 701 such configured as described above, the data controller 706 instructs the memory controller 705 in starting the transfer of the image data, and thus, allows the memory controller 705 to read the accumulated image data from the image memory 704 in sequence. The read image data is restored into an

original signal by the facsimile image processor 703, followed by density changing processing and scaling processing, to be input into the data controller 706.

The image data input into the data controller 706 is
5 encoded and compressed by the image compressor/decompressor
707, is modulated by the modem 708, and then, is sent to
a destination via the network controller 709. The image
information which has been already transmitted is erased
from the image memory 704.

10 At the time of reception, a received image is
accumulated once in the image memory 704. At this time,
if the received image can be recorded and output, the image
is recorded and output at the timing of completion of the
reception of the image by an amount of one sheet. Otherwise,
15 when the facsimile transmitter/receiver 701 is called during
a copying operation to start the reception, the received
image is accumulated in the image memory 704 until a using
ratio of the image memory 704 reaches a predetermined value,
for example, 80%. When the using ratio of the image memory
20 704 reaches 80%, the writing operation performed at that
time is forcibly interrupted, so that the received image
is read out of the image memory 704 to be thus recorded and
output.

At this time, the received image read out of the image
25 memory 704 is erased from the image memory 704. The

interrupted writing operation is resumed at the time when the using ratio of the image memory 704 is decreased down to, e.g., 10%. Upon completion of the entire writing operation, the remaining received image is recorded and
5 output. Moreover, in order to resume the writing operation after the interruption, various parameters for the writing operation during the interruption are internally saved. At the time of resuming the writing operation, the parameters are internally restored.

10 Next, unit configuration of the image processing apparatus in the present embodiment will be explained. Fig. 8 is a block diagram illustrating one example of the unit configuration when the image processing apparatus is a digital combined machine.

15 As illustrated in Fig. 8, in case of the digital combined machine, the image processing apparatus comprises three units: the image reading unit 101, an image engine control unit 800 and the image writing unit 104, each of the three units being managed on an independent PCB
20 substrate.

The image reading unit 101 consists of a CCD 801, an A/D converting module 802 and a gain control module 803, for converting optical image information, which has been optically read, into a digital image signal.

25 The image engine control unit 800 consists of mainly

the system controller 231, the process controller 211 and
the memory module 222 contained inside the image memory
control unit 102, wherein the image processor 204, the image
memory access controller 221 and the image data controller
5 203 in charge of the bus control are managed as a single
unit.

Furthermore, the image writing unit 104 consists of
mainly the video data controller 205, and includes the image
forming unit 206.

10 In the above-described unit configuration, when the
specifications and performance of the image reading unit
101 are modified, it is sufficient that only the image reading
unit 101 is modified in the system of the digital combined
machine, thereby making it unnecessary to modify the other
15 units since the data interfaces are held. Moreover, when
the image forming unit (engine) 206 is modified, the system
can be reconstructed by modifying only the image writing
unit 104.

In this manner, since the units dependent on the
20 input/output devices construct the system with the
independent configurations, the system can be graded up by
only replacing the minimum unit as long as the data interfaces
are held.

In the configuration of the image engine control unit
25 800 illustrated in Fig. 8, the respective modules (the

constituents) of the image processor 204, image data controller 203 and image memory access controller 221 are independent of each other. Consequently, the transfer from the image engine control unit 800 to the controller signifies
5 the removal of an unnecessary module, and therefore, a common module is used for general-purpose use. In this manner, the similar function is fulfilled by using the common module without independently configuring the module for the image engine control and the module for the controller.

10 Subsequently, the image data compression performed by the image processing apparatus in the present embodiment will be explained. Although an explanation will be given below on the configuration and operation of the data compressor 403 inside the image data controller 203 (see
15 Fig. 4), the data compressor 606 inside the image memory access controller 221 (see Fig. 6) or the image compressor/decompressor 707 inside the facsimile transmitter/receiver 701 may be configured in a similar manner according to a mode to be used.

20 First of all, configuration and operation of the data compressor 403 will be explained. Fig. 9 is a block diagram illustrating the configuration of the data compressor 403 in the image processing apparatus in the present embodiment; and Fig. 10 is a timing chart illustrating the processing
25 timings of the data compressor 403.

In Fig. 9, the data compressor 403 comprises: a line memory group 901 for storing image data therein; a compressor 902 for compressing the image data; an output switch 903 for inputting the image data and switching its output destination; and an input switch group 904 for switching an input source in the line memory group 901 and connecting it to the compressor 902.

Furthermore, the line memory group 901 includes an obverse line memory group 901a consisting of a plurality of FIFO memories FM1a, FM2a and FM3a for storing obverse image data therein, and a reverse line memory group 901b consisting of a plurality of FIFO memories FM1b, FM2b and FM3b for storing reverse image data therein.

The output switch 903 includes an obverse output switch 903a for switching the output destination of the obverse image data, and a reverse output switch 903b for switching the output destination of the reverse image data. Out of the output switches 903a and 903b, the obverse output switch 903a switches the output destination of the input image data among the FIFO memories FM1a, FM2a and FM3a and a through line TL4a serving as a circuit for transmitting the image data directly to the compressor 902. In the same manner, the reverse output switch 903b switches the output destination of the input image data among the FIFO memories FM1b, FM2b and FM3b and a through line TL4b.

The input switch group 904 includes an input switch 9041 for switching the FIFO memories FM1a and FM1b, an input switch 9042 for switching the FIFO memories FM2a and FM2b, an input switch 9043 for switching the FIFO memories FM3a and FM3b, and an input switch 9044 for switching the through lines TL4a and TL4b. Here, the FIFO memory used in the line memory group 901 is a 1-port FIFO memory.

Incidentally, for the sake of simple explanation, a region to be compressed by the compressor 902 is assumed to be a rectangular region consisting of four pixels per line multiplied by four lines, i.e., four pixels in the main scanning (pixel) direction and four lines in the sub scanning (line) direction, as illustrated in Fig. 18. According to a mode to be used, a region to be compressed by the compressor 902 may consist of eight pixels per line multiplied by eight lines in the DCT (Discrete Cosine Transformation) used in the MPEG (Motion Picture Expert Group) system in the motion compression standard. That is, the size of the region to be compressed depends upon hardware or application to be used, and therefore, it is not particularly limited to the size of four pixels per line multiplied by four lines.

First, how the obverse image data is compressed will be explained. As illustrated in Fig. 10, the obverse image data which has been output from the image processor 204 is first input via the obverse image data input controller 402a

in compressing the image data. The image data are sequentially input into the obverse output switch 903a. The obverse output switch 903a transmits the image data consisting of first four pixels, for example, pixels P11, P12, P13 and P14 illustrated in Fig. 18 (image data on a first line of the obverse) to the FIFO memory FM1a.

When image data on a next pixel (i.e., a fifth pixel, or P21) is to be input, the obverse output switch 903a switches the output destination to the FIFO memory FM2a, and then, transmits image data consisting of four pixels including the above-described pixel (image data on a second line of the obverse) to the FIFO memory FM2a. In the same manner, when image data on a ninth pixel (P31) is to be input, the obverse output switch 903a switches the output destination to the FIFO memory FM3a, and then, transmits image data consisting of four pixels including the above-described pixel (image data on a third line of the obverse) to the FIFO memory FM3a.

When image data on a next 13th pixel (P41) is to be input, the obverse output switch 903a switches the output destination to the through line TL4, and then, transmits image data consisting of four pixels including the above-described pixel (image data on a fourth line of the obverse) directly to the compressor 902 via the input switch 9044. Simultaneously, the image data on the first to third

lines of the obverse respectively stored in the FIFO memories FM1a to FM3a are read under the control of the command controller 410, and then, are transmitted to the compressor 902 via the input switches 9041, 9042 and 9043, respectively
5 (see Fig. 10).

The compressor 902 receives the image data on the obverse of the first to third lines, and then, compresses them as a single unit. With the above-described operation, the image data consisting of the four pixels per line
10 multiplied by the four lines can be compressed as a single unit. The compressed data is output to the image processor 204 under the control of the command controller 410.

In the meanwhile, when the image data on a 17th pixel is to be input, the obverse output switch 903a switches the
15 output destination of the image data to the FIFO memory FM1a, and then, transmits image data on a fifth line to the FIFO memory FM1a. The obverse output switch 903a sequentially transmits image data on sixth and seventh lines to the FIFO memories FM2a and FM3a, respectively. The obverse output
20 switch 903a transmits image data on an eighth line directly to the compressor 902 via the input switch 9044. Simultaneously, the obverse output switch 903a transmits the image data on the fifth, sixth and seventh lines of the obverse respectively stored in the FIFO memories FM1a, FM2a
25 and FM3a to the compressor 902 via the input switches 9041,

9042 and 9043, respectively.

Hereinafter, the repetition of the similar control can achieve smooth compression of the obverse image data sequentially transmitted from the image processor 204. On the other hand, reverse image data also can be smoothly compressed in the same manner as the obverse image data. As described above, the command controller 410 controls the output switch 903, so that FIFO memories for the image data on the obverse and reverse can be saved by two lines in total, thereby reducing the size of the apparatus.

Furthermore, the data compressor 403 may be configured in such a manner as to share the compressor 902. Such a configuration can be achieved by controlling the storing timing of the obverse and reverse image data to be transmitted to the FIFO memories. First, at a timing t1, the image data on the first line of the obverse is input. The obverse output switch 903a transmits the image data to the FIFO memory FM1a under the control of the command controller 410. The FIFO memory FM1a writes the transmitted obverse image data.

At a timing t2, the obverse output switch 903a transmits, to the FIFO memory FM2a, the image data on the second line of the obverse input in sequence. At this time, the reverse output switch 903b transmits the input image data on the first line of the reverse to the FIFO memory FM1b.

Namely, the image data on the obverse and the image

data on the reverse are transmitted to the respective FIFO memories at the image data storing timings shifted by one line. An image data transmitting delay of one line can be generated by inserting a line memory equivalent to one FIFO memory in, for example, a front stage of the reverse output switch 903b.

At a timing t4, all of the input sources of the input switch group 904 are switched to the obverse line memory group 901a under the control of the command controller 410, and thus, the image data on the first to fourth lines of the obverse are transmitted to the compressor 902, which then compresses the image data on all of the four lines as a single unit.

In the same manner, since the reverse image data can be compressed as a single unit at a timing t5, the command controller 410 switches all of the input sources of the input switch group 904 to the reverse line memory group 901b, and thereafter, the image data on the first to fourth lines of the obverse are transmitted to the compressor 902, which then compresses the image data on all of the four lines as a single unit.

In this way, only one compressor can compress the obverse and reverse image data by shifting the input timing with respect to the compressor by one line, unlike in the prior art in which two compressors are required to compress

the obverse and reverse image data. Furthermore, the provision of the input switch group 904 can halve the circuit configuration after the output stage of the input switch group 904. That is, both of the obverse and reverse can
5 be read at a high speed in the reduced circuit size in the image processing apparatus in the present embodiment.

Incidentally, although the image processor 204 (see Fig. 2) includes the obverse image processor 204a and the reverse image processor 204b in the above-described
10 embodiment, the image processor may be only one according to a mode to be used, for example, when the processing capacity of a section serving as the image processing unit 103 (see Fig. 1) is enhanced.

Fig. 11 is a block diagram illustrating another example
15 of the configuration of the image processing apparatus when a single image processor 1101 is used; and Fig. 12 is a block diagram illustrating one example of the configuration of the image processor 1101.

As illustrated in Fig. 12, obverse image data and
20 reverse image data are input into the image processor 1101 from the image data controller 203, and therefore, a scanner image processor 1201 includes an obverse scanner image processor 1201a for scanning obverse image data and a reverse scanner image processor 1201b for scanning reverse image
25 data. With this configuration, the number of terminals for

chips can be reduced, thereby reducing the size of the circuit and the size of the apparatus.

As described above, the processing circuit can be shared in the image processing apparatus in the present embodiment by shifting the timings of the obverse image data processing and the reverse image data processing, so that the processing circuit can be reduced, and further, both of the obverse and reverse of the document can be read at the same time. Namely, only one compressor can compress the obverse and reverse image data by shifting the input timings with respect to the compressor by one line. Furthermore, the provision of the input switch can halve the circuit configuration after the output stage of the input switch.

A second embodiment of the present invention relates to a digital combined machine in which a bus is shared thereby simplifying the circuit configuration. The same component elements as those in the first embodiment are designated by the same legends, and to avoid repetition of matter, their description will be omitted.

Fig. 13 is a block diagram illustrating one example of the hardware configuration of an image processing apparatus in the second embodiment. The image processing apparatus 1301 comprises component elements for processing image data on an obverse and a reverse, respectively: an

obverse reading unit 201a, a reverse reading unit 201b, an
obverse sensor board unit 202a, a reverse sensor board unit
202b, an obverse image data controller 203a, a reverse image
data controller 203b, an obverse image processor 204a and
5 a reverse image processor 204b.

The image processing apparatus 1301 illustrated in
Fig. 13 merely exemplifies the hardware configuration of
the image processing apparatus in the present embodiment,
and therefore, the reading units and the like are not
10 necessarily configured in such a manner that the processing
of the obverse and the processing of the reverse are
independent of each other.

In the image processing apparatus 1301, the obverse
image data controller 203a and the reverse image data
15 controller 203b for respectively controlling flows of the
obverse and reverse image data are connected to a common
parallel bus 220. Consequently, the obverse and reverse
image data can be transmitted or received via a single bus.

Like the image processing apparatus in the first
20 embodiment, the image processing apparatus 1301 is
configured per functional unit, and thus, a memory module
222 for storing the image data or the like therein is included
inside the image memory control unit 102 independent of the
image data control unit 100, to which the image data
25 controller 203 pertains (see Fig. 1). Consequently,

compressed image data need be transmitted via a parallel bus 220.

In the conventional image processing apparatus, the obverse image data and the reverse image data are transmitted
5 via the buses independent of each other inside the motherboard 1511 (see Fig. 15), i.e., the obverse image transfer bus 1515a and the reverse image transfer bus 1515b, respectively. Therefore, the size of the apparatus has been inevitably increased. However, in the image processing
10 apparatus 1301 in the present embodiment, the controllers are connected to the single bus (i.e., the parallel bus 220), thereby reducing the size of the circuit.

At this time, since the obverse image data and the reverse image data are not distinguished from each other
15 on the parallel bus 220, the obverse image data controller 203a and the reverse image data controller 203b add identifying data to the image data. Fig. 14A and Fig. 14B illustrate the image data added with the identifying data.

In Fig. 14A, the identifying data is a memory address
20 itself. The memory module 222 as the storing destination is divided into an area for storing the obverse image data therein and an area for storing the reverse image data therein. In other words, the memory module 222 is divided into the area for storing the obverse image data therein and the area
25 for storing the reverse image data therein, and the

identifying data is adapted to designate the storing destination.

In contrast, in Fig. 14B, the identifying data for determining whether the image data is the obverse image data or the reverse image data is added next to the memory address of the storing destination.

As illustrated in Fig. 14A, high-speed memory storing processing can be achieved by determining whether or not it is the obverse image data in each area of the storing destination; in contrast, no waste occurs in the memory by adding an identifier, as illustrated in Fig. 14B.

Thus, since the single bus is used for inputting/outputting the obverse image data and the reverse image data in the image processing apparatus in the present embodiment, the processing circuit can be reduced in size, unlike the prior art in which the two buses are required via the motherboard. Furthermore, since the image data is added with the identifying data, it is easy to determine whether the image data is the obverse image data or the reverse image data.

As described above, according to one aspect of the present invention, the reading unit simultaneously reads the image data on both of the obverse and reverse of the document; the compressing unit subjects the image data to the compressing processing; and the controlling unit

controls the timings at which the image data on both of the obverse and reverse of the document are transmitted to the compressing unit in such a manner as to generate the difference in timing between the processing of compressing the obverse image data read by the reading unit and the processing of compressing the reverse image data read by the reading unit. Consequently, the processing circuit can be shared by shifting the timings of the image processing of the obverse image data and the image processing of the reverse image data, thus producing the effect of providing the image processing apparatus in which the processing circuit can be reduced in size, and further, both of the obverse and reverse of the document can be read at the same time.

According to another aspect of the present invention, the reading unit simultaneously reads the image data on both of the obverse and reverse of the document; the storing unit stores therein the image data read by the reading unit; the compressing unit subjects the image data stored in the storing unit to the compressing processing; and the controlling unit controls the storing unit so as to perform, out of the image data to be compressed by the compressing unit, the processing of compressing the obverse image data and the processing of compressing the reverse image data at the different timings. Consequently, it is possible to

share the compressing unit for performing the processing
of compressing the obverse image data and the processing
of compressing the reverse image data, thus producing the
effect of providing the image processing apparatus in which
5 the processing circuit can be reduced in size, and further,
both of the obverse and reverse of the document can be read
at the same time.

According to still another aspect of the present
invention, the reading unit simultaneously reads the image
10 data on both of the obverse and reverse of the document;
the data dividing unit divides, out of the image data read
by the reading unit, each of the obverse image data and the
reverse image data into the image data consisting of $m \times$
 n pixels, i.e., m pixels per line multiplied by n lines;
15 the storing unit stores therein the image data divided by
the data dividing unit; the compressing unit compresses the
image data consisting of $m \times n$ pixels as a single unit; the
switch unit connects the storing unit and the compressing
unit to each other and switches the image data to be input
20 into the compressing unit between the obverse image data
and the reverse image data; and the transmission controlling
unit controls the transmission of the image data consisting
of $m \times (n-1)$ pixels out of the image data consisting of m
 $\times n$ pixels divided by the data dividing unit to the storing
25 unit, the transmission of the image data on the residual

one line directly to the compressing unit, and further, the transmission of the image data consisting of $m \times (n-1)$ pixels stored in the storing unit to the compressing unit. Consequently, it is possible to share the compressing unit
5 for performing the processing of compressing the obverse image data and the processing of compressing the reverse image data, and to reduce the volume of the image data stored in the storing unit, thus producing the effect of providing the image processing apparatus in which the processing
10 circuit can be reduced in size, and further, both of the obverse and reverse of the document can be read at the same time.

According to still another aspect of the present invention, the reading unit simultaneously reads the image
15 data on both of the obverse and reverse of the document; the obverse image processing unit subjects the obverse image data out of the image data read by the reading unit to the image processing; the reverse image processing unit means subjects the reverse image data out of the image data read
20 by the reading unit to the image processing; the appending unit adds the identifying information for identifying whether the image data read by the reading unit is the obverse image data or the reverse image data; and the communication line connects the obverse image processing unit and the
25 reverse image processing unit to each other, wherein the

communication line is used in transmitting or receiving the
image data. Consequently, it is possible to identify
whether the image data read by the reading unit is the obverse
image data or the reverse image data, and to transmit or
5 receive the obverse and reverse image data via the single
data bus without any necessity of providing a data bus for
each of the obverse processing and the reverse processing,
thus producing the effect of providing the image processing
apparatus in which the processing circuit can be reduced
10 in size, and further, both of the obverse and reverse of
the document can be read at the same time.

The present document incorporates by reference the
entire contents of Japanese priority documents, 2000-023132
filed in Japan on January 31, 2000.

15 Although the invention has been described with respect
to a specific embodiment for a complete and clear disclosure,
the appended claims are not to be thus limited but are to
be construed as embodying all modifications and alternative
constructions that may occur to one skilled in the art which
20 fairly fall within the basic teaching herein set forth.